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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,729	03/30/2004	Hsien-Ping Feng	TS03-636	4817

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EXAMINER	
LE, DUNG ANH	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,729	FENG ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *31-39* is/are withdrawn from consideration.

5)☒ Claim(s) *30* is/are allowed.

6)☒ Claim(s) *1-8,13-18,20-22,27 and 28* is/are rejected.

7)☒ Claim(s) *9-12,19,23-26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DLe

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 3/30/04 is acceptable.

Election/Restriction

Application's election without traverse of Group II (Claims 1-30), drawn to process of making a semiconductor device is acknowledged for prosecution in the subject application . Applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims.

Applicants are reminded to cancelled non-elective claims.

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 5/6/2004 and made of record . The references cited on the PTOL 1449 form have been considered.

Drawings

The drawings are objected to for the following reason:

Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid

abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 112

Claim 5 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, line 1, the language of " said metal " is insufficient antecedent basis for this limitation in the claim, claim 1 provides the antecedent basic for this term. It is not clearly "said metal" refers to "first metal" or second metal".

Set of claims 1-13:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3- 6 and 13 are rejected under 35 USC 102 (b) as being anticipated by Ueno (6,221,765 B1).

Ueno teaches a method of forming a metal interconnect in an opening formed on a substrate (fig. 4, Embodiment 1, col 7, line 37)), comprising:

(a) providing a substrate 1 with an opening 5 formed therein, said opening has sidewalls, a top, and a bottom;

(b) forming a seed layer 4 within said opening 5;

(c) forming a first metal layer 6 on said seed layer 4 by a first electrochemical plating (ECP) process to partially fill said opening;

(d) performing a first anneal step (col 7, line 61);

(e) forming a second metal layer 7 on said first metal layer 6 with a second ECP process to fill said opening; and

(f) performing a second anneal step (col 8, line 8).

Regarding claim 3, a diffusion barrier layer 3 on the sidewalls and bottom of said opening prior to forming a seed layer 4.

Regarding claim 4, wherein said diffusion barrier layer 3 (col 7, line 45) has a thickness of about 200 to 500 Angstroms and is comprised of one or more of Ta, TaN, Ti, TiN, TaSiN, W, and WN.

Regarding claim 5, wherein said metal is copper 6 and the seed layer 4 is comprised of copper with a thickness between about 1000 and 2000 Angstroms.

Regarding claim 6, wherein said first ECP process is performed at a temperature between about 10°C to 20°C and with a current density of about 5 to 15 mA/cm2 (col 7, line 62).

Regarding claim 13, a CMP process following said second anneal wherein said second metal layer becomes coplanar with the top of the opening (col 8, line 23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 7-8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Ueno in view of the following remark.

Ueno teaches the claimed invention as applied to claim 1, except for further comprised of a cleaning process between steps (c) and (d) and between steps (e) and (f) as cited in current claim.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform a cleaning process between steps (c) and (d) and between steps (e) and (f) in order to prepare surface for annealing steps.

Regarding claims 7-8, Ueno teaches the claimed invention as applied to claim 1, including annealing temperature range 300° C or higher (col2, line 37), but Ueno does not teach first and second anneal steps are performed in a process chamber at a temperature between about 180°C and 260°C for a period of about 10 to 200 seconds in a reducing gas or inert gas environment and wherein the reducing gas is H2 or NH3 as cited n current claims.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply first and second anneal steps are performed in a process chamber at a temperature between about 180°C and 260°C for a period of about 10 to 200 seconds in a reducing gas or inert gas environment and wherein the reducing gas is H2 or NH3, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Set of claims 14-29

Claims 14-18, 20-22, 27-28 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Ueno in view of Kunishima et al. (2005/0095847 A1).

Ueno teaches a method of forming a copper interconnect in an opening formed in a stack of dielectric layers on a substrate, comprising:

(a) providing a substrate with a stack of dielectric layers formed thereon;

(b) forming an opening in said stack of dielectric layers, said via and trench each having sidewalls, a top, and a bottom;

(c) depositing a conformal diffusion barrier layer on the sidewalls and bottoms of said opening and depositing a seed layer on the diffusion barrier layer;

(d) depositing a first copper layer on the seed layer by a first electrochemical plating (ECP) process that partially fills said opening;

(e) performing a first anneal step;

(f) depositing a second copper layer on said first copper layer with a second ECP process, said second copper layer fills said opening;

(g) performing a second anneal step; and

(h) planarizing said second copper layer to be coplanar with the top of the stack of dielectric layers.

Ueno does teach opening (damascene) having sidewall, bottom and a top. Ueno does not teach opening comprised of a via and an overlying trench in said

stack of dielectric layers, said via and trench each having sidewalls, a top, and a bottom as cited in current claim.

Kunishima et al. teach opening comprised of a via and an overlying trench in said stack of dielectric layers, said via and trench each having sidewalls, a top, and a bottom as set forward in figs. 8a-9e and [0146].

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form opening comprised of a via and an overlying trench in said stack of dielectric layers, said via and trench each having sidewalls, a top, and a bottom in Ueno 's structure/method, in order to obtain various applications of the interconnection structure.

Regarding claim 15, Ueno and the above remark teach the claimed invention as applied to claim 14, except for further comprised of a cleaning process between steps (c) and (d) and between steps (e) and (f) as cited in current claim.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform a cleaning process between steps (c) and (d) and between steps (e) and (f) in order to prepare surface for annealing steps.

Regarding claim 16, diffusion barrier layer 6 has a thickness of about 200 to 500 Angstroms and is comprised of one or more of Ta, TaN, Ti, TiN, TaSiN, W, and WN.(col 7, line 46).

Regarding claim 17, seed layer is comprised of copper and has a thickness between about 1000 and 2000 Angstroms (col 7, line 48).

Regarding claim 18, Ueno in view of Kunishima et al. disclose opening comprises trench and via, but fail to disclose the distance from the top of the trench to the bottom of the via is about 4000 to 13000 Angstroms as cited in the present claim .

However, it would have been obvious to one having ordinary skill in the art making semiconductor device to determine the workable or optimal range for the distance from the top of the trench to the bottom of the via is about 4000 to 13000 Angstroms through routine experimentation and optimization to optimal device performance.

Regarding claim 20, first ECP process is performed at a temperature of about 10°C to 20°C (col 7, line 63) and with a current density of about 5 to 15 mA/cm2.

Regarding claim 21 the first and second ECP processes are performed in the same work piece and include an electrolyte solution comprised of $CuSO_4$, HCl, and one or more organic additives (col 7, line 56 and col 8, line 5).

Regarding claim 22, Ueno teaches the claimed invention as applied to claim 14, including annealing temperature range 300° C or higher (col2, line 37), but Ueno does not teach first and second anneal steps are performed in a process chamber at a temperature between about 180°C and 260°C for a period of about

10 to 200 seconds in a reducing gas or inert gas environment and wherein the reducing gas is H2 or NH3 as cited n current claim.

Regarding claim 27, wherein planarizing said second copper layer involves a chemical mechanical polish process (col 8, line 23).

Regarding claim 28, Ueno in view of Kunishima et al. discloses the claimed invention as applied to claim 14, except for further comprised of a third ECP process followed by a third anneal step after the second anneal step and before said planarizing step.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply a third ECP process followed by a third anneal step after the second anneal step and before said planarizing step since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

Reasons for Indication of Allowable Subject Matter

Claims 9- 12, 19, 23-26 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ueno (U.S. Patent No. 6221765 B1), Kunishima et al. (2005/0095847 A1) and Background of Invention, taken

individually or in combination, do not teach the claimed invention having **(Regarding claims 9 and 23)** first anneal step is performed in a PECVD process chamber with a H2 plasma treatment comprised of a H2 flow rate between about 5 and 10 sccm, a RF power of about 200 to 400 Watts, a chamber pressure of about 0.1 to 10 Torr, and a chamber temperature from about 150°C to 350°C for a period of about 10 to 200 seconds; **(Regarding claims 10 and 24)** second anneal step is performed in a PECVD process chamber with a H2 plasma treatment comprised of a H2 flow rate between about 1 and 10 sccm, a RF power of about 300 to 400 Watts, a chamber pressure of about 0.1 to 10 mTorr, and a chamber temperature from about 150°C to 400°C for a period of about 10 to 200 seconds, **(Regarding claims 11 and 25)** the second ECP process is comprised of a first deposition step having a current density of 20 to 60 mA/cm2 and a second deposition step having a current density of about 60 to 100 mA/cm2, **(Regarding claim 19)**. The method of claim 14 wherein the first ECP process fills the via and about half of-the trench and **(Regarding claim 29)** the second ECP process is performed with a current density of about 40 mA/cm2 and the third ECP process deposits a third copper layer on the second copper layer and is performed with a current density of about 60 mA/cm2.

Claim 30 would be allowed. The following is a statement of reason for the indication of allowable subject matter:

Claim 30 is considered allowable since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ueno (U.S. Patent No. 6221765 B1), Kunishima et al. (2005/0095847 A1) and Background of Invention, taken individually or in combination, do not teach the claimed invention having the steps of performing a second anneal step; depositing a third copper layer on said second copper layer with a third ECP process, said third copper layer overfills said trench; and performing a third anneal step.

If Applicants are aware of better art than that which has been cited, they are required to call such to attention of the examiner.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE DL
Primary Examiner
Art Unit 2818